Modeling systems via register machines

for the verification of weak memory models

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Why WMMs?

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Simplify the model!

Register Machines

Assume a set Θ of threads, a set $\mathcal{V}$ of variables, and a set $\mathtt{Regs}$ of registers, the values of which range over some domain $\mathcal{D}$.

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- $(\mathsf{W}, \theta, x, a)$ – Thread θ writes to variable x, storing the value in register a.
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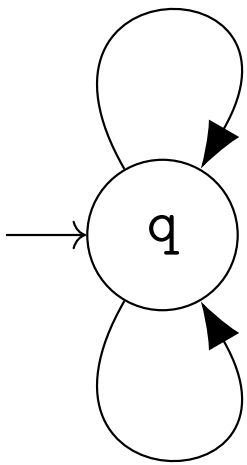
Definition (Register Machine)

A *register machine* $\mathcal{M}$ is a tuple $\langle Q, q_{\mathtt{init}}, \Delta \rangle$, where Q is the (finite) set of states, $q_{\mathtt{init}} \in Q$ is the initial state, and Δ is the finite set of transitions, where each $t \in \Delta$ is of the form $\langle q, \mathsf{o}, q' \rangle$ where $q, q' \in Q$ are states and o is an operation.

Example: Instantaneous visibility

$(\mathrm{R}, \theta, x, a) + (\mathrm{W}, \theta, x, a)$



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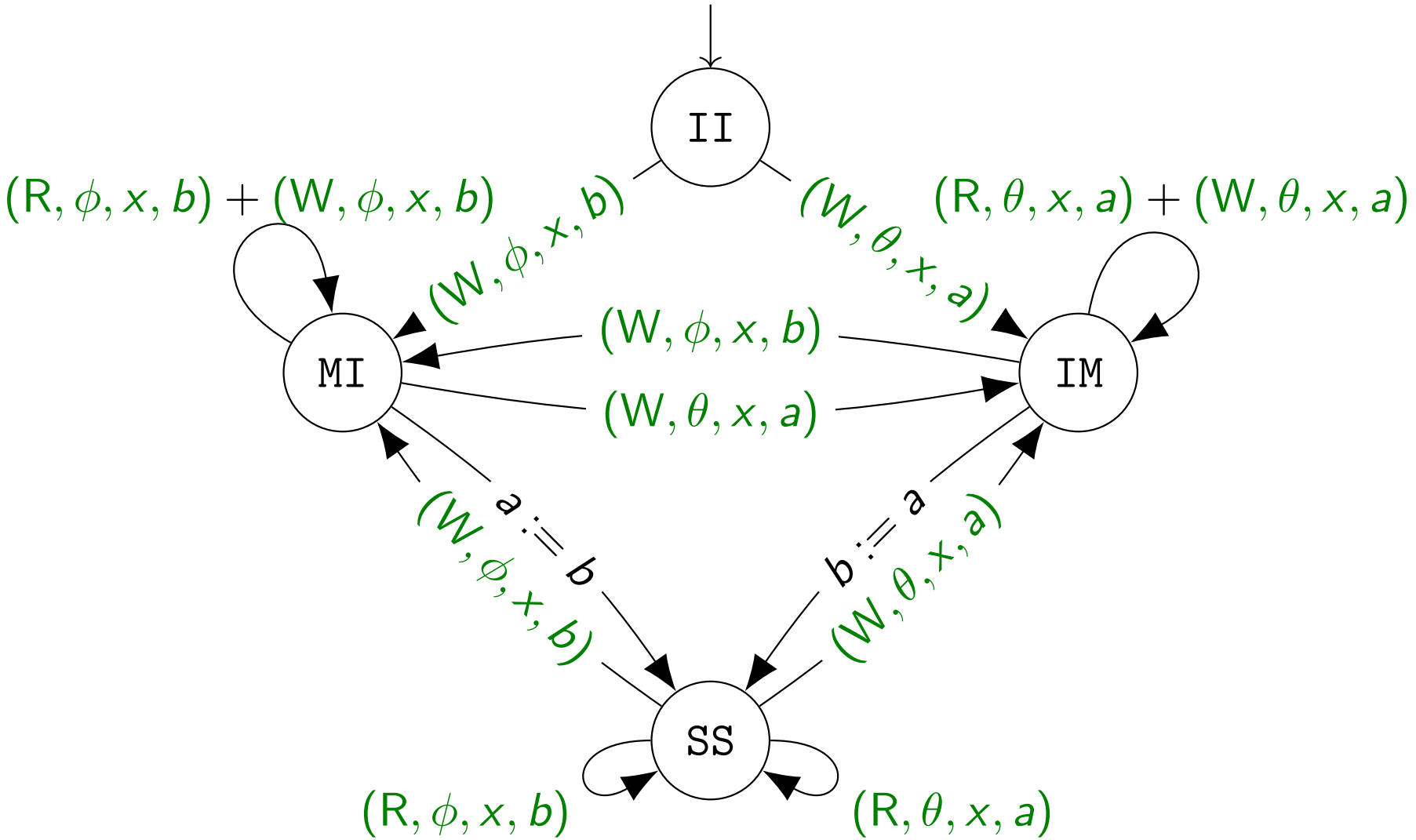
Example: MSI Protocol



Thread-local Memory

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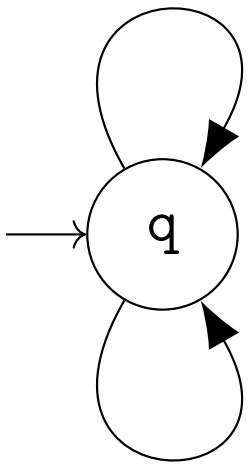

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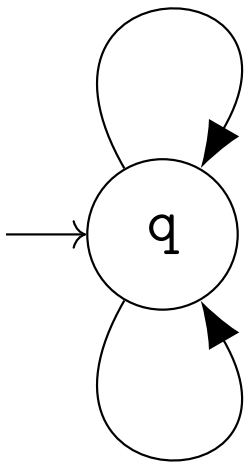

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Writes are instantly visible to all threads!

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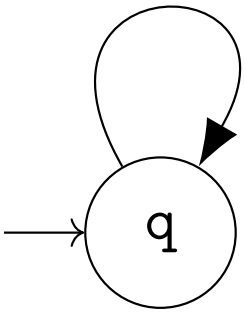

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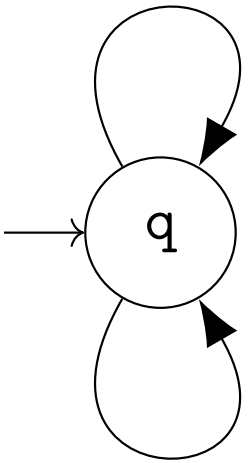

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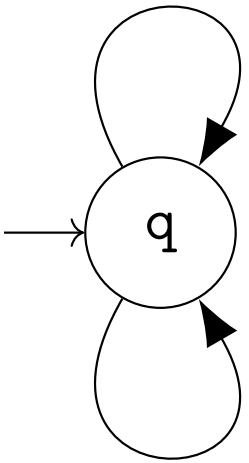

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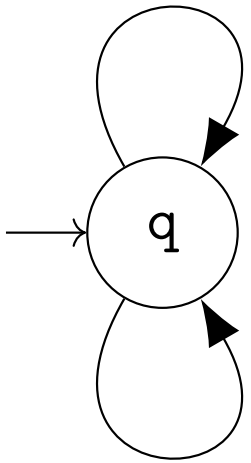

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Solution: Encode information about whether a written value has been passed to shared memory.

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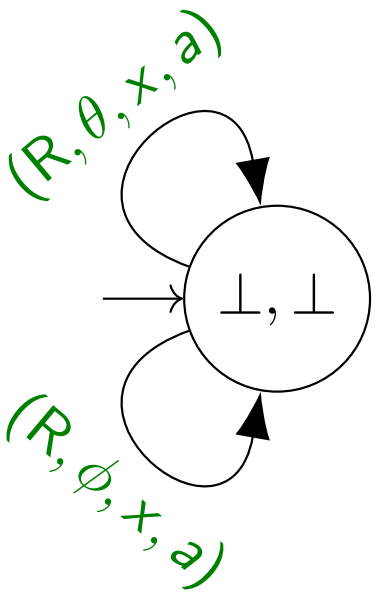

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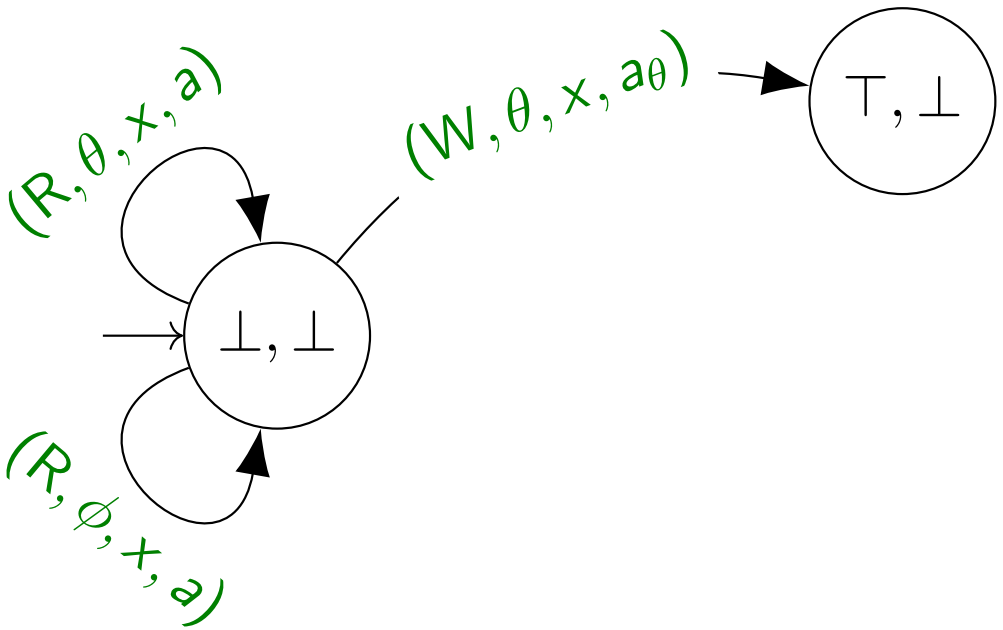

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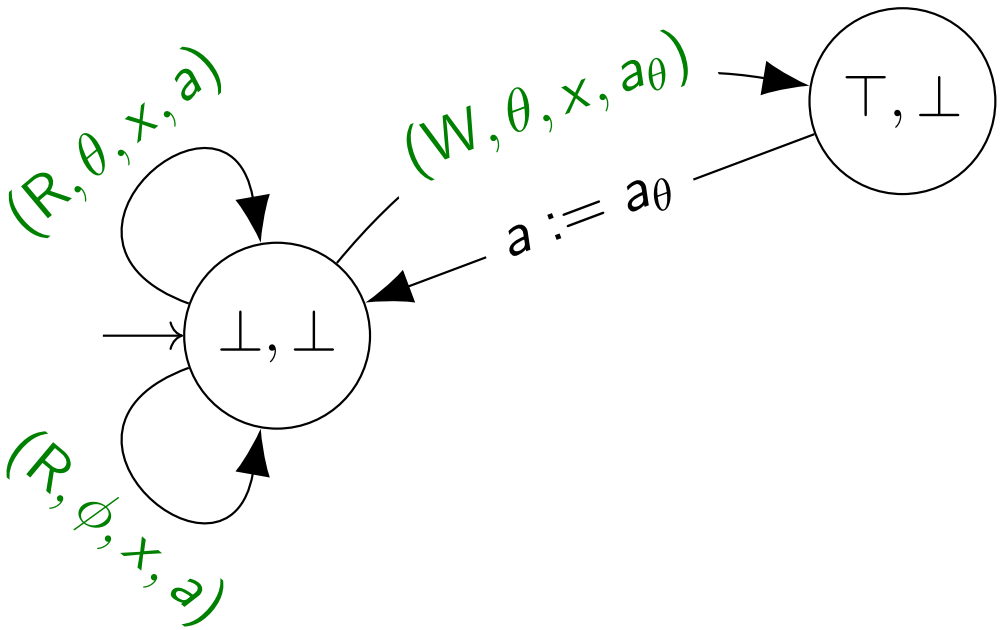

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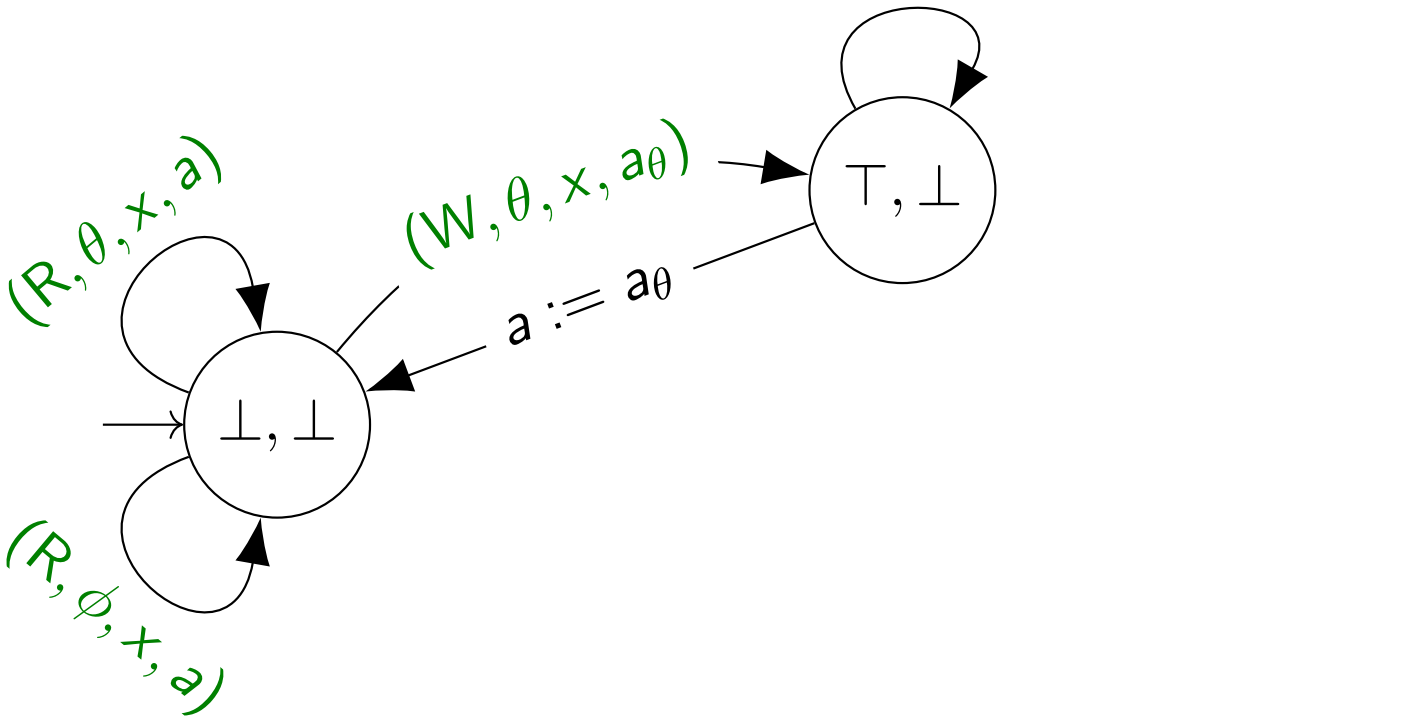

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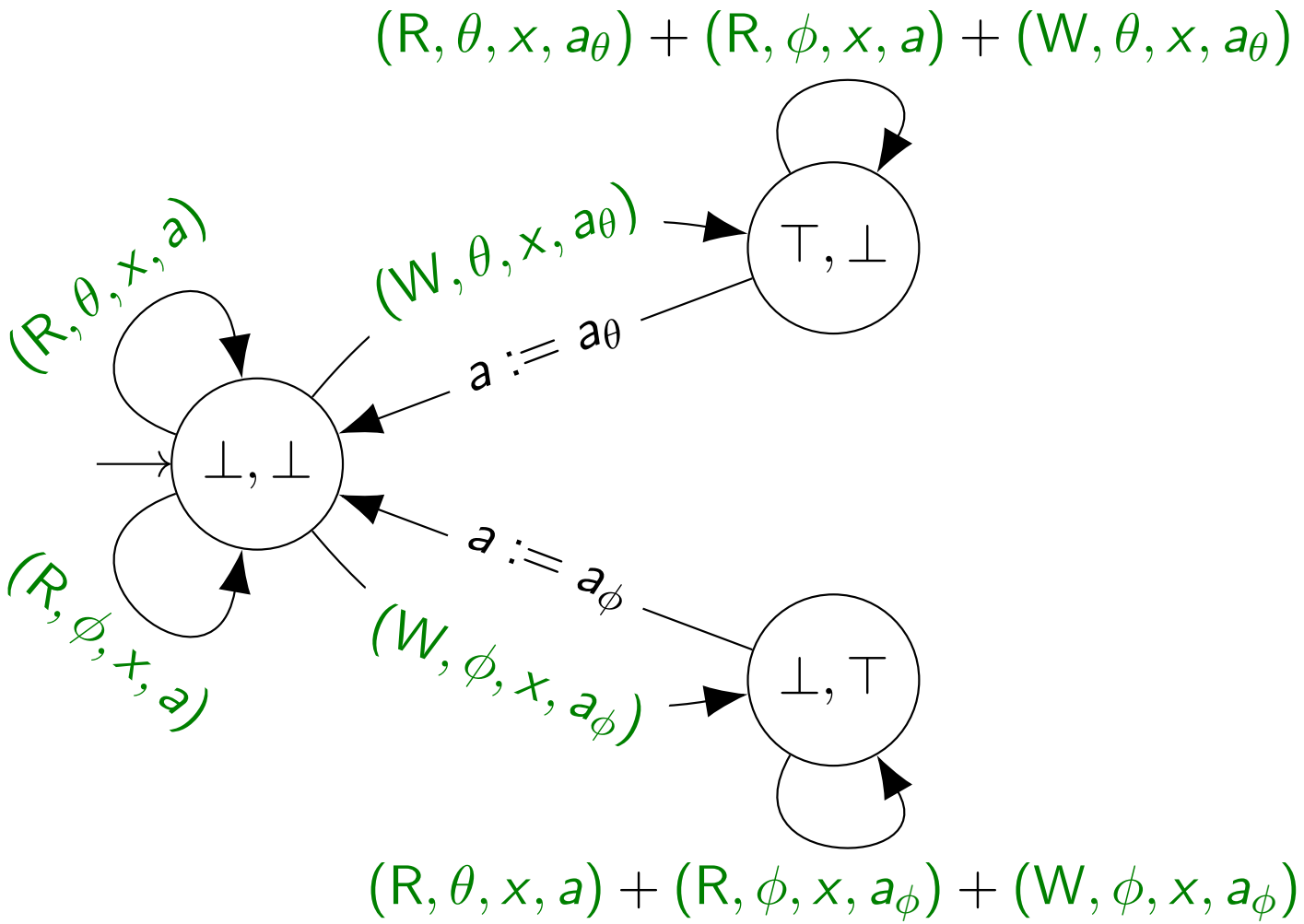

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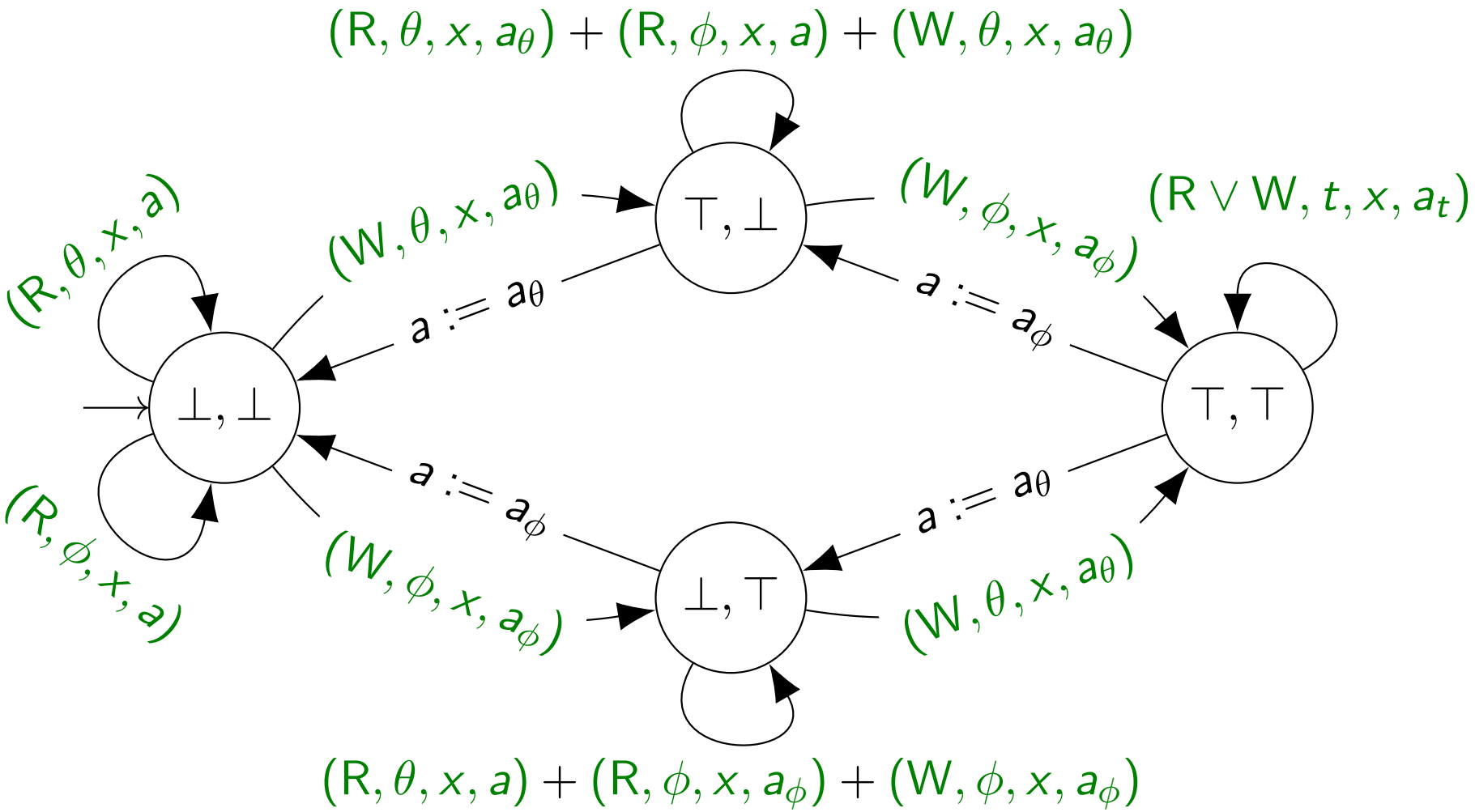

Buffers

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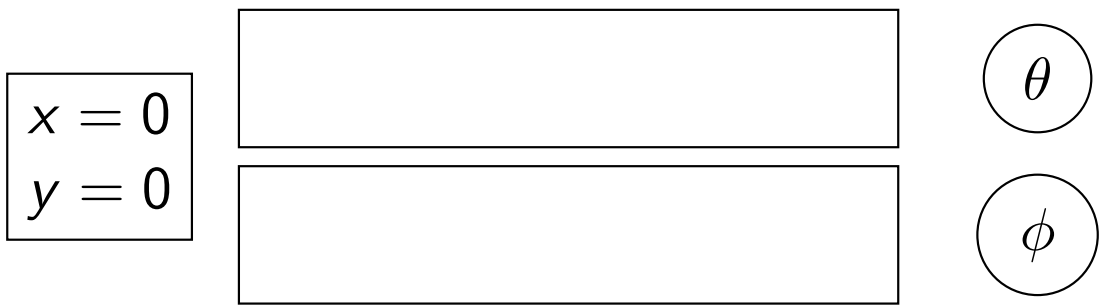
- Writes that are not immediately visible to all threads (e.g. `TSO` write- or load buffer semantics)
- Delays due to traveling time in distributed systems (e.g. message queues)

TSO-style Store Buffers



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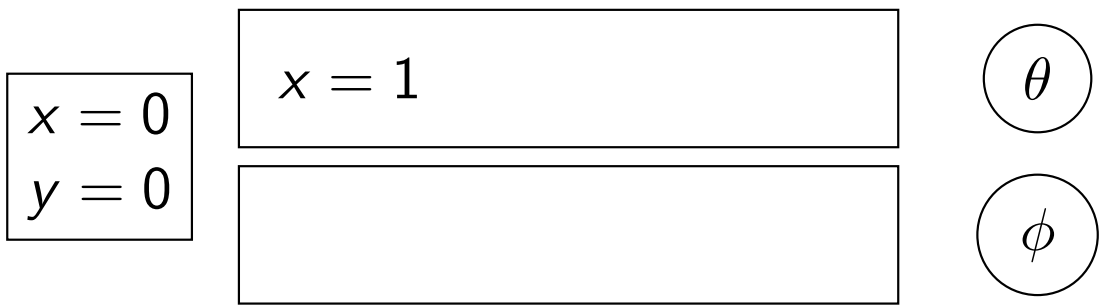

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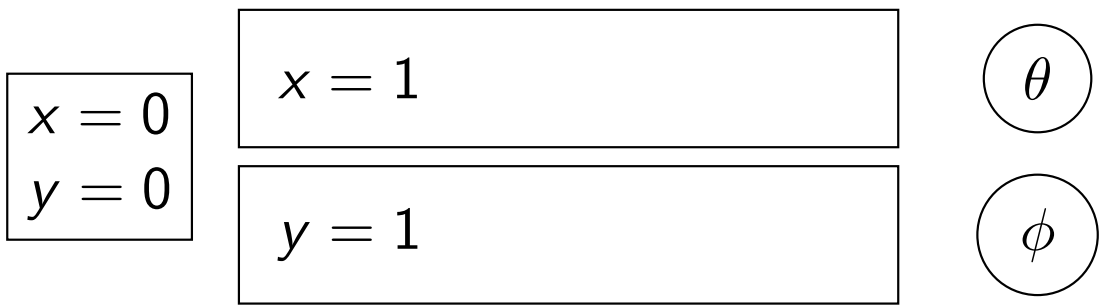

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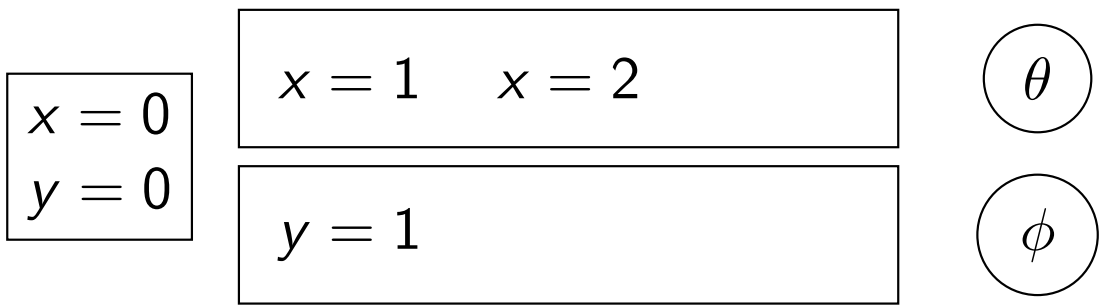

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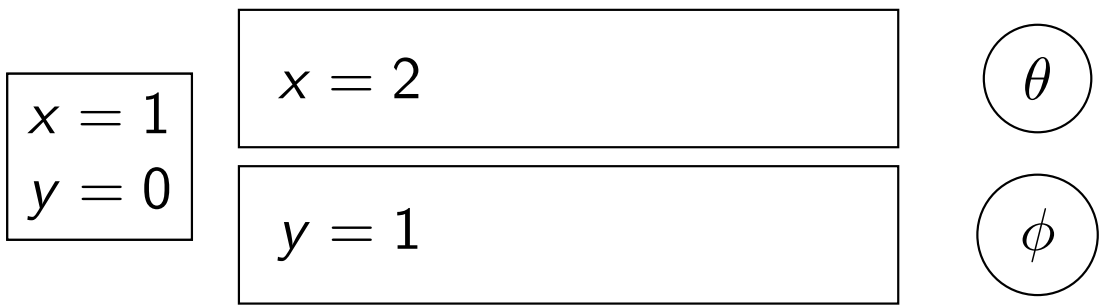

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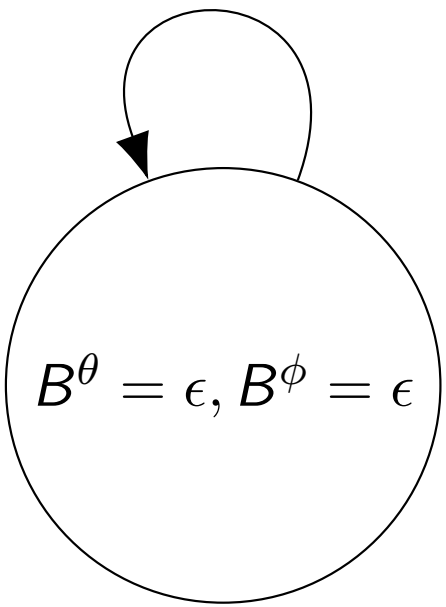

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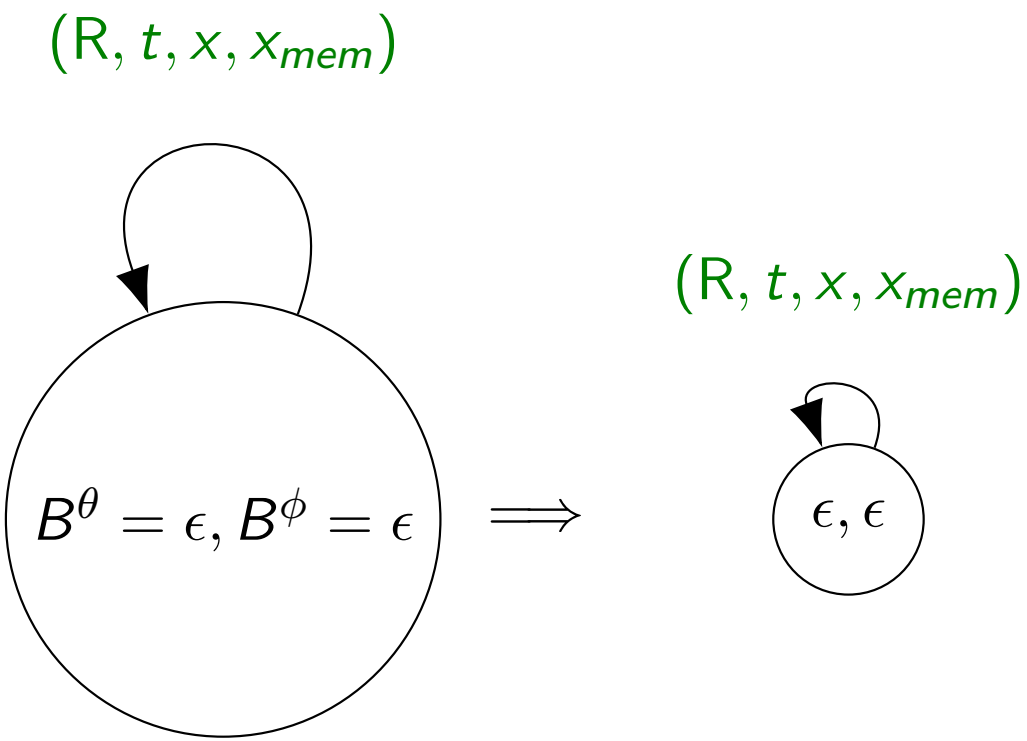

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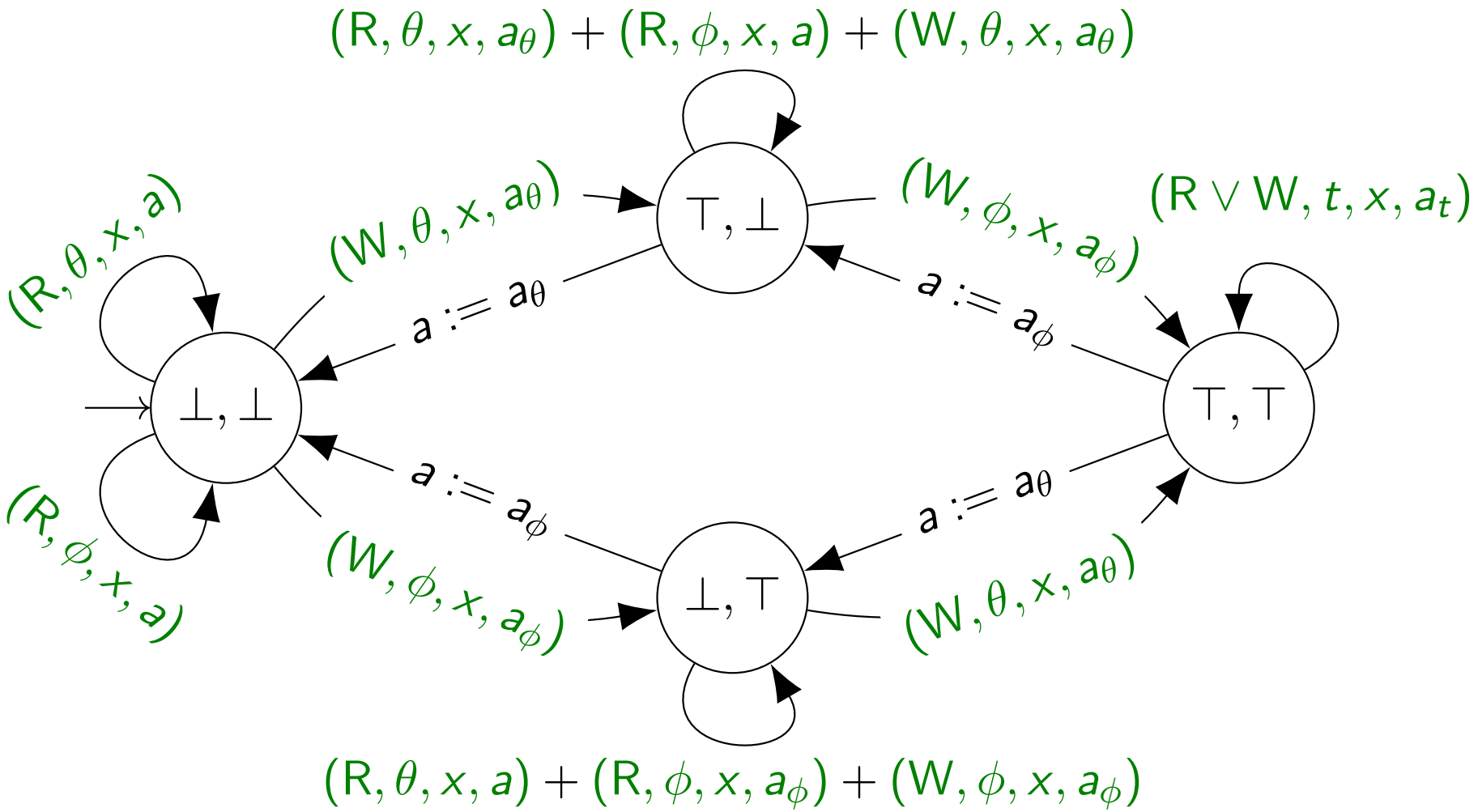

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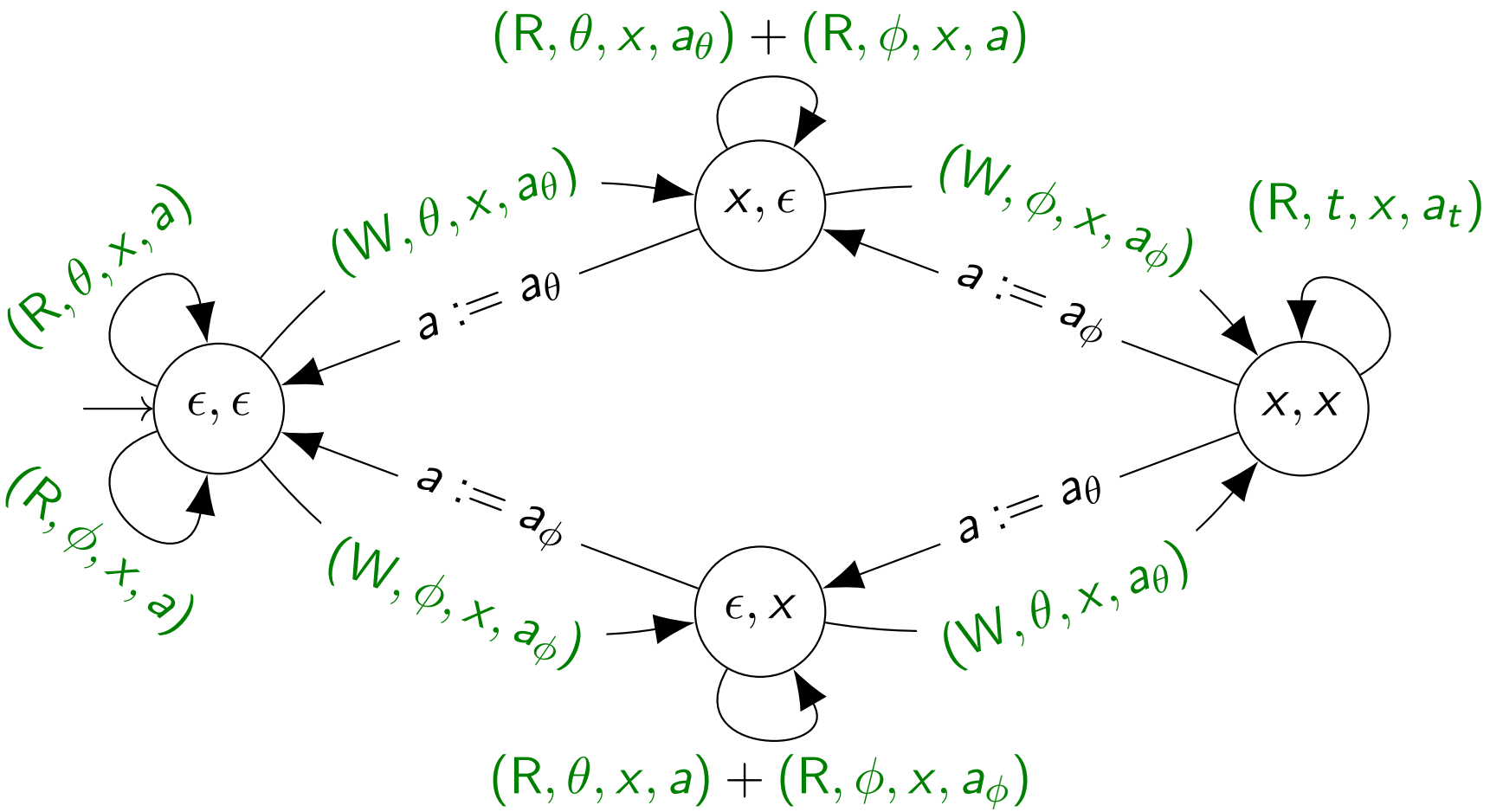
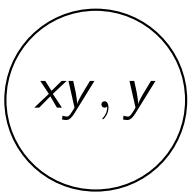


TSO-style Store Buffers: Read/Write

Writing and reading



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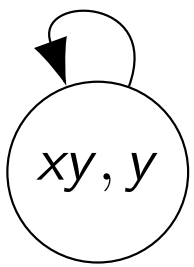

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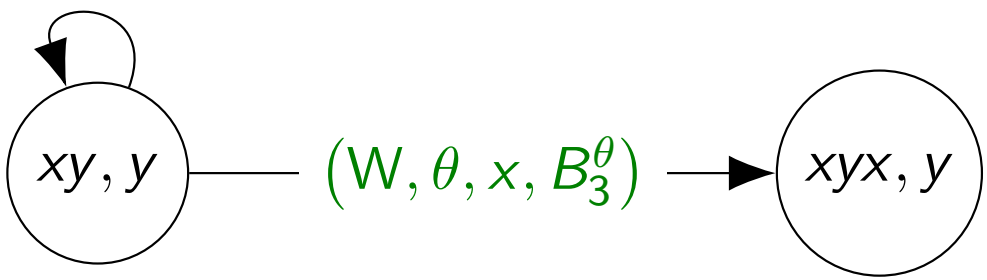

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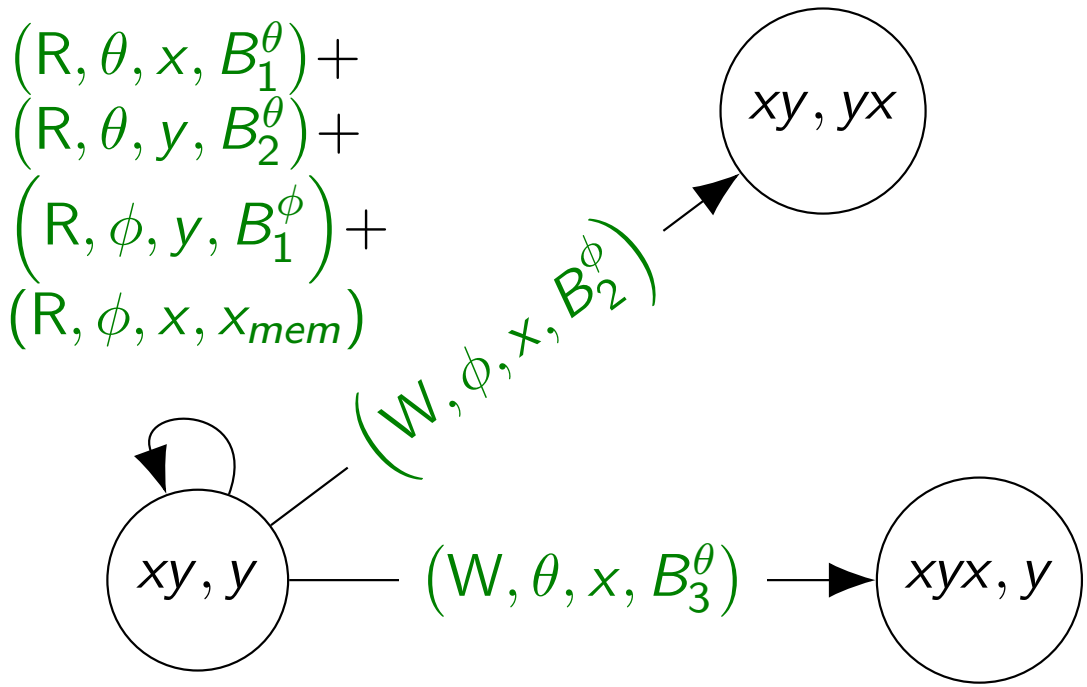
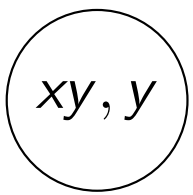


TSO-style Store Buffers: Handling message



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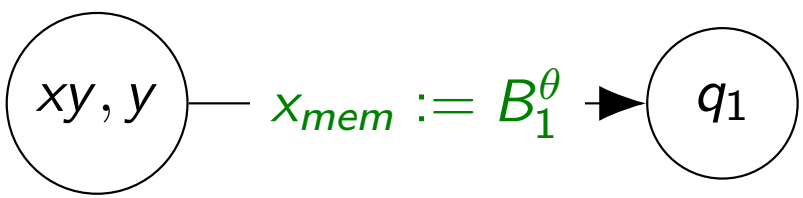

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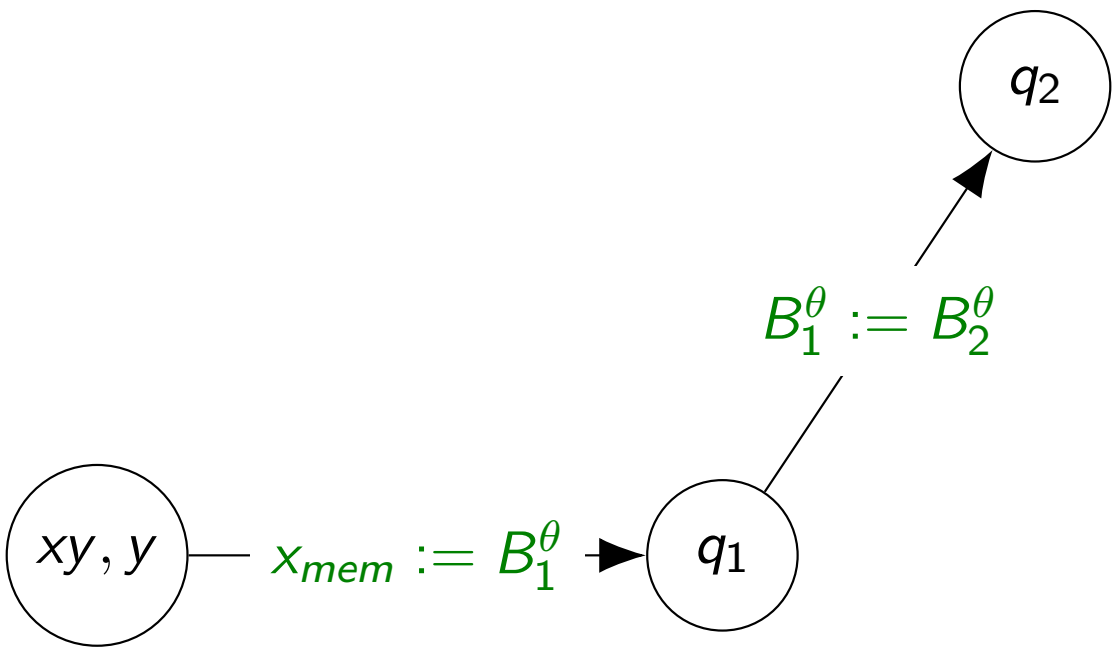

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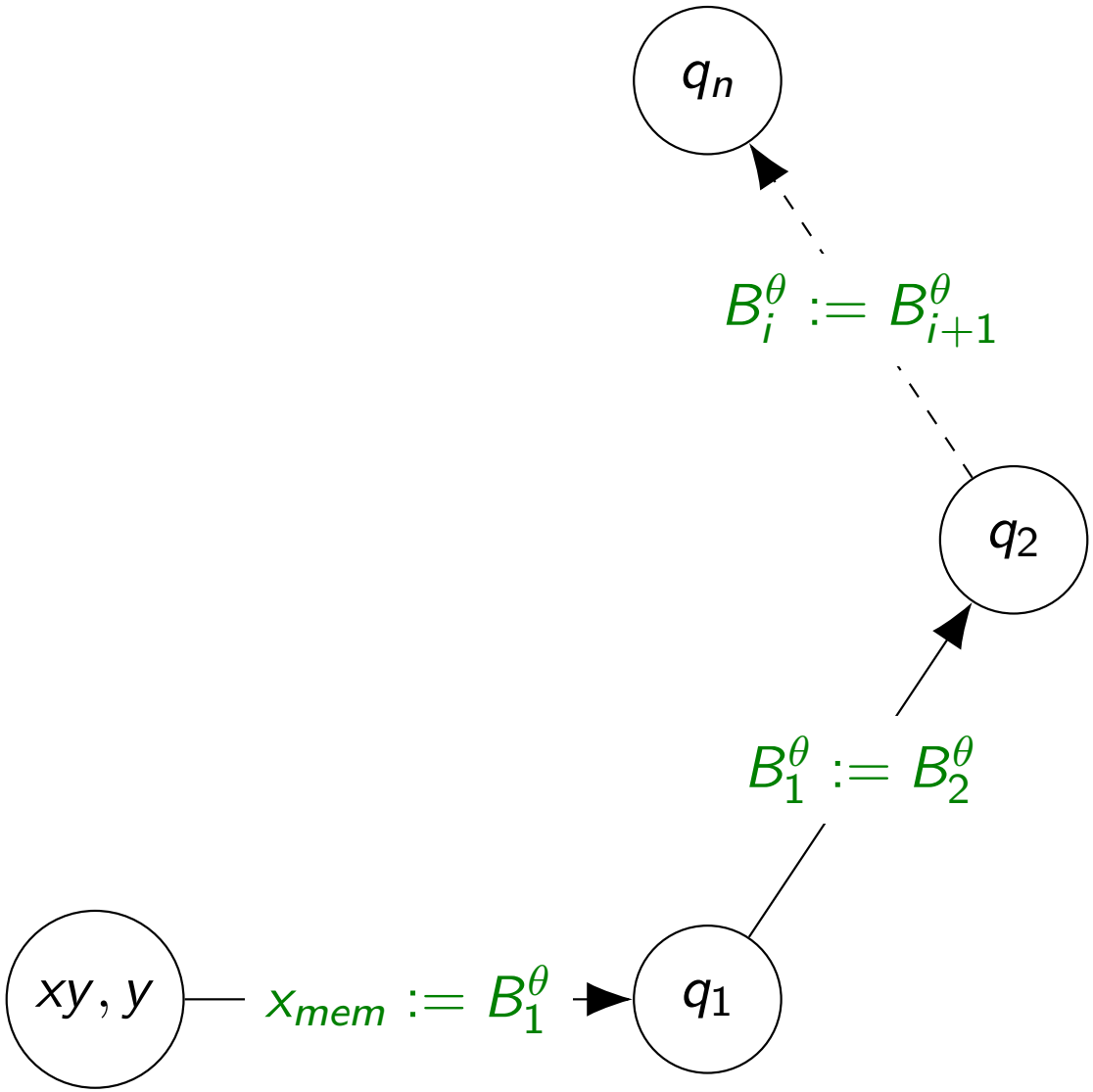

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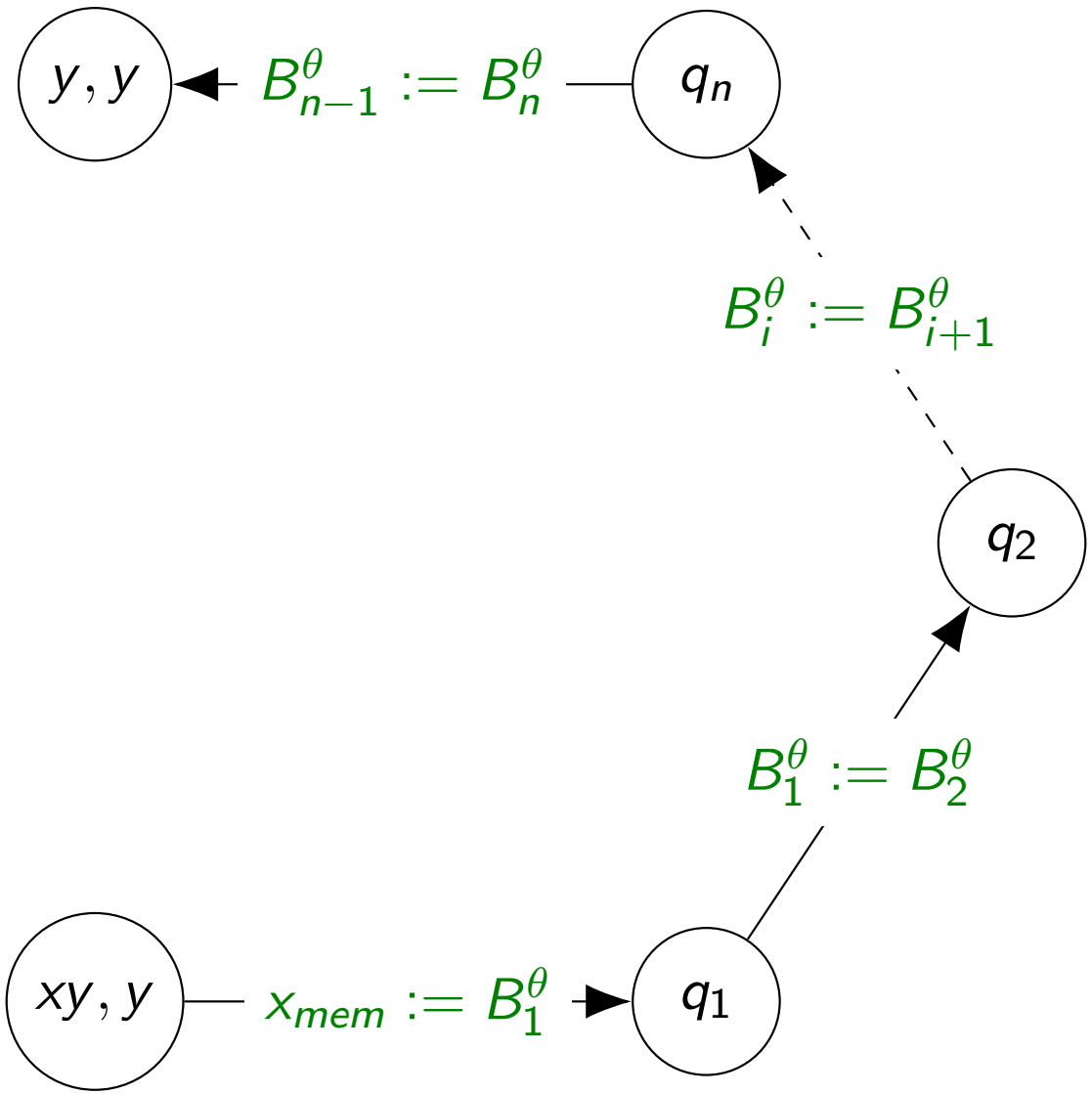

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- Otherwise, we have a dummy transition $q \xrightarrow{a:=a} q'$.

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2. Exponential growth (state explosion) – not ideal, but OK.

However: We have decidability for more memory models, and we can still model useful systems!

References

[1] Ahmed Bouajjani, Constantin Enea, Rachid Guerraoui, and Jad Hamza.
On verifying causal consistency.
In Giuseppe Castagna and Andrew D. Gordon, editors, *Proceedings of the 44th ACM SIGPLAN Symposium on Principles of Programming Languages, POPL 2017, Paris, France, January 18-20, 2017*, pages 626–638. ACM, 2017.